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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,781	06/26/2003	Masanari Yokogawa	047297-0136	4070

22428 7590 06/14/2005

FOLEY AND LARDNER  
SUITE 500  
3000 K STREET NW  
WASHINGTON, DC 20007

EXAMINER
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ALEJANDRO MULERO, LUZ L

ART UNIT	PAPER NUMBER
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1763

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/603,781

**Applicant(s)**

YOKOGAWA ET AL.

**Examiner**

Luz L. Alejandro

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

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## **DETAILED ACTION**

### ***Drawings***

Figures 3-6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki et al., U.S. Patent 5,460,684.

Saeki et al. shows the invention substantially as claimed including a semiconductor wafer treatment member having at least a surface formed with a silicon carbide film 3 thereon, comprising a support portion for supporting a semiconductor wafer, said support portion being composed of salients with which said semiconductor wafer substantially comes into contact; and depressions formed with the silicon carbide film to provide a coverage area between said salients, said salients being formed with a surface roughness of 0.1 to 1.5 microns (see fig. 1 and its description).

Saeki et al. does not expressly disclose the salients being formed with a surface roughness of 0.05 to 1.3 microns, wherein said coverage area has a ratio of 20 to 90% to a total area of said depressions, the depressions having faces with a roughness of 3 microns or more when measured for a length of 300 microns, and the top surfaces of the salients and said surfaces of the depression have boundary portions in the form of curves. With respect to the surface roughness of the salients, a prima facie case of obviousness exists because overlapping ranges establish a prima facie case of obviousness. Regarding the coverage area ratio, the roughness of the depressions, and the boundaries between the salients and depression, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum coverage ratio and surface roughness based upon a variety of factors including the desired degree of adhesion to the wafer, for example, and such limitation would not lend patentability to the instant invention absent a showing of unexpected results. Concerning the shape of the boundaries, the configuration of the claimed boundaries is a matter of choice which a person of ordinary skill in the art would

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have found obvious absent persuasive evidence that the claimed boundary shape is significant.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toya et al., U.S. Patent 5,200,157 in view of Saeki et al., U.S. Patent 5,460,684.

Toya et al. shows the invention substantially as claimed including a semiconductor wafer treatment member having at least a surface formed with a silicon carbide film 2 thereon, comprising a support portion for supporting a semiconductor wafer, said support portion being composed of salients with which said semiconductor wafer substantially comes into contact; and depressions formed with the silicon carbide film to provide a coverage area between said salients, said salients being formed with a surface roughness of 12.5 microns (see fig. 3 and its description).

Toya et al. does not expressly disclose a silicon carbide film, the salients being formed with a surface roughness of 0.05 to 1.3 microns, wherein said coverage area has a ratio of 20 to 90% to a total area of said depressions, and the top surfaces of the salients and said surfaces of the depression have boundary portions in the form of curves.

Saeki et al. discloses a support with a silicon carbide film 3 thereon (see fig. 1 and its description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Toya et al. so as to include a silicon carbide film as shown in Saeki et al. because this is shown to be a suitable wafer support structure.

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Regarding the coverage area ratio, the roughness of the salients, and the boundaries between the salients and depression, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum coverage ratio and surface roughness based upon a variety of factors including the desired degree of adhesion to the wafer, for example, and such limitation would not lend patentability to the instant invention absent a showing of unexpected results. Concerning the shape of the boundaries, the configuration of the claimed boundaries is a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the claimed boundary shape is significant.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waldhauer et al., US 2004/0060512.

Waldhauer et al. shows the invention substantially as claimed including a semiconductor wafer treatment member having at least a surface formed with a silicon carbide film 134 thereon, comprising a support portion for supporting a semiconductor wafer, said support portion being composed of salients with which said semiconductor wafer substantially comes into contact; and depressions formed with the silicon carbide film to provide a coverage area between said salients, said salients being formed with a surface roughness of 4-16 microinches which equates to 0.106-0.4064 microns (see fig. 3 and its description).

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Waldhauer et al. does not expressly disclose the salients being formed with a surface roughness of 0.05 to 1.3 microns, wherein said coverage area has a ratio of 20 to 90% to a total area of said depressions, the depressions having a surface roughness of 3 microns or more when measured for a length of 300 microns, and the top surfaces of the salients and said surfaces of the depression have boundary portions in the form of curves. With respect to the surface roughness of the salients, a prima facie case of obviousness exists because overlapping ranges establish a prima facie case of obviousness.

Regarding the coverage area ratio, the roughness of the salients, and the boundaries between the salients and depression, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum coverage ratio and surface roughness based upon a variety of factors including the desired degree of adhesion to the wafer, for example, and such limitation would not lend patentability to the instant invention absent a showing of unexpected results. Concerning the shape of the boundaries, the configuration of the claimed boundaries is a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the claimed boundary shape is significant.

### ***Conclusion***


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luz L. Alejandro whose telephone number is 571-272-

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1430. The examiner can normally be reached on Monday to Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Luz L. Alejandro  
Primary Examiner  
Art Unit 1763

June 10, 2005